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Compact Switched Capacitor Multilevel Inverter (CSCMLI) With Self Voltage Balancing and Boosting Ability

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***Abstract:* - This letter presents a compact switched capacitor multilevel inverter topology with reduced switch count and with self-voltage balancing and boosting ability. The operational mode of proposed CSCMLI is discussed. A comparative analysis in terms of number of switches and blocking voltages is presented against recent switched capacitor multilevel inverter topologies. Further to enhance the quality of the output voltage, a new level shifted multicarrier PWM modulation technique is recommended. This modulation technique produces low THD and high rms voltage. The proposed modulation technique is implemented in the nine-level CSCMLI with single dc source and two capacitors. The simulated and experimental results are verified for a switching frequency of 50Hz and 2.5 kHz using the proposed PWM control.**

Index Terms: cascaded multilevel inverter, single-stage capacitor module, PWM technique, voltage boosting, voltage balancing

I. INTRODUCTION

The design of converters for renewable energy system is another challenge for power electronics researchers. The widely installed renewable energy sources such as photovoltaic, wind and fuel cell are highly participating in energy conversion [1]. Multilevel inverters are playing major role in these energy conversion systems. These inverters comprise of dc source, active switches, series of capacitors and power diodes. The conventional multilevel inverters such as neutral point clamped, flying capacitor and cascaded H-bridge are predominantly used in medium to high voltage applications. The cascaded H-bridge topology has unique advantages like modularity and lower number of power components [2-3]. Even though, the conventional topologies have more features like modularity and low *dv/dt* stress, it suffers from the use of more number of active and passive devices and also balancing of capacitor voltages are still challenging. To minimize the drawbacks of conventional topologies, recent multilevel inverters are presented in [4]-[11]. The objectives of these topologies are to minimize the number of dc source, active switches and self-balancing of capacitor voltages. The high frequency cascaded inverter for grid connected PV and electric vehicle is proposed with reduced switching frequency in [4]. Each unit consists of six active switches, a diode, a dc source and a capacitor. The capacitor charging and discharging is done through proper switching sequence with single source to generate five level stepped output voltage. The reduced switch count with self-voltage balancing of series and parallel connection of capacitor is presented in [5]. The fundamental and high frequency modulation technique for the proposed topology is compared in terms of power losses.

A new voltage step-up structure with self-balancing is discussed in [6].The capacitors are charged in first two states and discharged in the next two states to produce the nine-level output voltage. To increase the level, the series connection of basic unit is also recommended. Another high step up voltage inverter with reduced switches and self-voltage balancing is presented in [7]. The proposed basic cell comprises of a capacitor, a diode and two switches. In each cycle, the series and/or parallel connection of capacitors are charged and discharged. However, the topology presented in [5]-[7] uses full bridge inverter as a second stage of conversion which has to block the high voltage, because it increases the *dv/dt* stress on the switches.

To minimize this *dv/dt* stresses without losing the other features of above inverters, the new multilevel inverters structures are presented in [8]-[11]. In [8], the single dc source without full bridge inverter is presented. This topology has lower *dv/dt* stress on individual switch, but the number of capacitors and active switches are increasing as the number of level increases. Hybrid switched capacitor inverter for two symmetric and asymmetric configurations are demonstrated in [9]-[10]. One switch & diode in each full bridge unit is added to charge the capacitor, but the number of switches are high as number of level increases. The single stage switched capacitor (S^3CM) module is demonstrated in [11] which is the modified version of topology presented in [6]. The main objective of S^3CM topology is to minimize the blocking voltage across the switches and it uses single dc source as the input, but the switch count is high.

To resolve the drawbacks of S^3CM, this letter presents a compact switched capacitor multilevel inverter (CSCMLI) topology with self-voltage balancing and boosting ability with reduced number of switches. The balancing of the voltages across the capacitors are achieved by choosing proper switching sequence to charge and discharge the capacitor. The capacitors are integrated to maintain the equal average voltage during the switching operation. Further to enhance the quality of output voltage, a new level shifted multicarrier PWM modulation scheme is presented. The features of proposed topology and modulation schemes are:

1) Total number of power components are reduced.
2) The maximum blocking voltage on individual switches is limited to $V_{in.}$
3) Due to less number of components, it reduces the number of on-state switches and power losses.
4) The voltages across the capacitors are self-balanced and the capacitor voltages (C_1&C_2) are independent of the load power factor.
5) The modulation scheme generates low harmonics and high RMS voltage compared to conventional PWM technique.

This letter is organized as follows: section II presents the construction of the proposed 9-level inverter with simple explanation on the various modes of operation with new modulation scheme and the generalized Fourier analysis. In Section III, the simulation and experimental results are discussed and section IV, brief the conclusion.

II. OPERATION OF PROPOSED CSCMLI TOPOLOGY

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The single phase circuit diagram of the proposed CSCMLI topology is depicted in Fig.1.It constitutes of single input dc source, two series connected dc-link capacitor, and eleven switches (IGBTs). The CSCMLI topology is able to generate a maximum of nine-level stepped voltage, but the number of output voltage can be extended to "m" level by cascading the basic unit of CSCMLI.

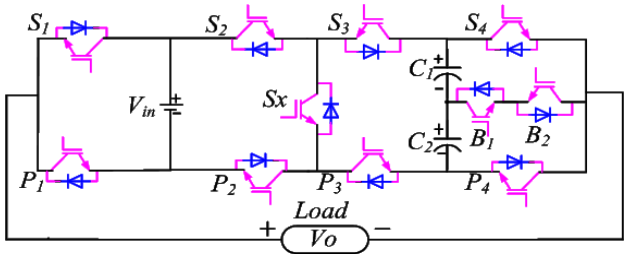

Fig.1 Proposed capacitor switched-9-level inverter module

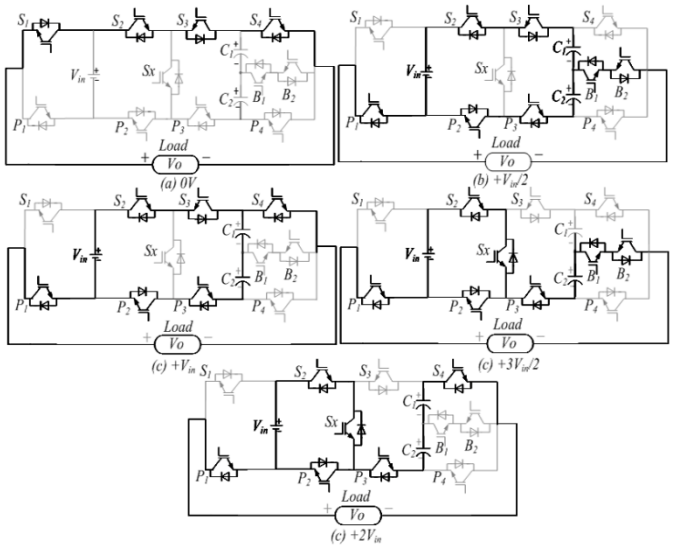

Fig.2(a)-(e) Mode operation for zero state and positive half cycle

TABLE.1 SWITCHING SEQUENCE OF EACH LEVEL FOR OUTPUT VOLTAGE WITH STATE OF CAPACITORS

State	On-State Switches	Output Voltage (V_o)	State Capacitors	
			V_{C1}	V_{C2}
0	S_1,S_2,S_3,S_4 / P_1,P_2,P_3 P_4,	0V	-	-
1	S_2,S_3,P_3,P_4,B_1,B_2 $S_1,S_2,S_3,P_2,P_3,B_1,B_2$	$+V_{in}/2$ $+ V_{in}/2$	C	C
2	S_2,S_3,S_4,P_1,P_2,P_3 S_1,S_2,S_3,P_2,P_3,P_4	$+ V_{in}$ $- V_{in}$		
3	S_2,P_1,P_3,S_x,B_1,B_2 S_1,S_3,P_2,S_x,B_1,B_2	$+3V_{in}/2$ $-3V_{in}/2$	D	D
4	S_2,S_4,P_1,P_3,S_x $S_1,S_3,P2,P_4,S_x$	$+2V_{in}$ $-2V_{in}$		

It is worth mentioning that the CSCMLI requires a maximum voltage rating on switches of V_{in} for *m*-level. The S_1-S_4&P_1-$P_4$are unidirectional switches with anti-parallel diode whereas the B_1-B_2 combinedly act as bidirectional switch *i.e* two IGBTs are connected in anti-series to allow the current to flow in both the directions and it has the maximum withstanding voltage of $0.5V_{in}$. The switch pairs (S_1, P_1), (S_2, P_2, S_x), (S_3, P_3, S_x) and (S_4, P_4) should not be turned on simultaneously to avoid the short circuits of the switches with dc source. The switch S_x is placed parallel to the dc source which provides the current path to discharge the capacitors in third and fourth state. The circuit structure of S^3CM has twelve switches but the proposed *CSCMLI* topology requires eleven switches which further reduces the logic gates of pulse generation signal, driver circuits and increases the overall power density. In order to generate the nine-level stepped output voltage level the switching sequence of each level is given in Table.1. Here, nine-level inverter is discussed and it has zero to four state of operation in positive and negative cycle. Initially, the capacitors (C_1&C_2) are charged to $V_{in}/2$ in state 1 and 2, the output voltage levels are $\pm V_{in}/2$ & $\pm V_{in}$. In state 3 and 4, the stored the capacitor voltages are discharged to load and the load values are $\pm 3V_{in}/2$ & $\pm 2V_{in}$ as illustrated in Fig.2 (a)-(e). In this way, the voltages are boosted by charging and discharging of capacitors. The charging and discharging of capacitors are done equally to balance the voltages. The upper capacitor value is higher than the lower voltage capacitor in [10], but here both the capacitors have equal values because the charging and discharging period is equal.

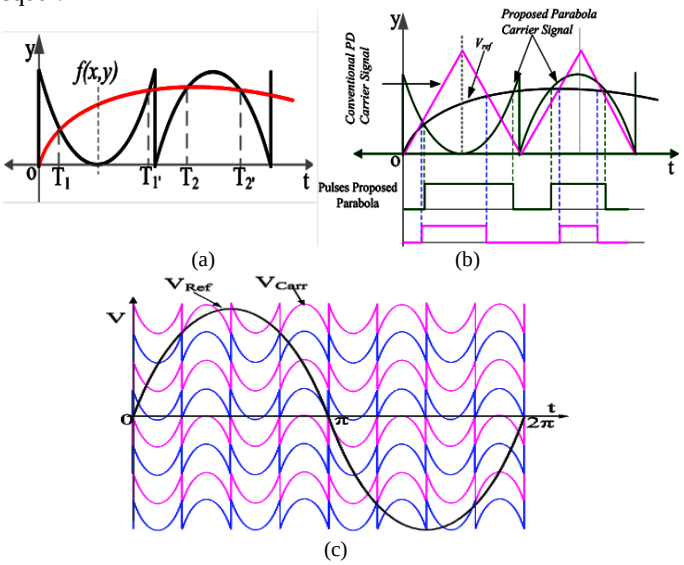

Fig. 3(a) proposed parabola carrier signal (b) conventional and proposed carrier signals with pulse width variations and (c) Level shifted proposed parabola carrier signal technique

To improve the output voltage rms and to minimize the voltage harmonics a new carrier signal PWM scheme is presented in this section. The proposed modulation strategy falls under the level shift modulation techniques (LS-PWM). The conventional level shift modulation technique is classified into (i) phase disposition (PD), (ii) phase opposite disposition (POD) and (iii) alternate phase opposite disposition (APOD). The proposed carrier is applicable to all three categories. The sideband harmonics are higher in the traditional PWM technique and to minimize the sideband harmonics, the carrier frequency to be high. This causes high electromagnetic interference, which affects the converter and its operation. This section presents a modified carrier signal with variation of pulse widths as shown in Fig.3 (a) and (b). The "*u-n*" wave is basically parabolic in nature, hence the variable controlled waveform *f (x,y)* as

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TABLE. 2 COMPARISON OF PROPOSED NINE-LEVEL INVERTER WITH CONVENTIONAL AND OTHER RECENT SCMLI TOPOLOGIES

Topologies	$N_{Switches}$	N_{Source}	$N_{Capacitors}$	$V_{C,rating}$	N_{Diode}	$MBV_{p.u}$	$TBV_{p.u}$	Capacitor Balancing	Voltage boosting Ability	Negative Level
NPC	16	1	8	$V_{in}/4$	56	V_{in}	16 V_{in}	Additional Circuits Required for >3-Level	No	via last two arms
FC	16	1	31	$V_{in}/4$	-			No additional Circuits Required	No	via last two arms
CHB	16	4	-	-	-			Not Applicable	-	via H-bridge
[4]	12	2	2	V_{in}	2	$2V_{in}$	20 V_{in}	Self Balancing	Yes	via H-bridge
[5]	8	1	3	V_{in}	6	$4V_{in}$	20 V_{in}			via H-bridge
[6]	10	1	2	V_{in}	1	$4V_{in}$	24 V_{in}			inherent
[7]	10	2	2	V_{in}	4	$4V_{in}$	20 V_{in}			via H-bridge
[8]	19	1	3	V_{in}	1	V_{in}	19 V_{in}			inherent
[9]	8	1	4	$2V_{in}$	1	$2V_{in}$	16 V_{in}			via H-bridge
[11]	12	1	2	$V_{in}/2$	1	V_{in}	12 V_{in}			inherent
Proposed	11	1	2	$V_{in}/2$	1	V_{in}	11 V_{in}			inherent

*MBV-Maximum Blocking Voltage on Individual Switches, TBV- Total Blocking Voltage of Switches

$$F(x,y)=\frac{A_{00}}{2}+\sum_{n=1}^{\infty}\left[A_{0n}\cos ny+B_{0n}\sin ny\right]+\sum_{m=1}^{\infty}\left[A_{0m}\cos mx+B_{0m}\sin mx\right]+\sum_{m=1}^{\infty}\sum_{\substack{m=-\infty\\(n\neq 0)}}^{\infty}\left[A_{mn}\cos(mx+ny)+B_{mn}\sin(mx+ny)\right] \quad (1)$$

where *m* is the carrier index variable and *n* is the baseband index variable. The above equation consists of fundamental component and baseband harmonics, carrier harmonics and sideband harmonics [12]. Since the *u-n* wave is parabolic in nature the *f(x,y)* function in the above equation can be replaced with x^2 and the fundamental Fourier equation for voltage is given as :

$$A_{00}+jB_{00}=\frac{2V_{dc}}{2\pi^2}\times\int_{-\pi}^{\pi}\left(1+\pi M\cos y\right)dy \quad (2)$$

Where 'M' is modulation index. By solving (2), the fundamental value is $A_{00}=2V_{dc}$, $B_{00}=0$ when double edge modulation is used. Since the duty cycle of each pulse is higher than the conventional PWM and the conduction time is high in parabolic PWM technique as shown in Fig.3(b) and generalized level shifted carrier signal (V_{Carr}) with sinusoidal reference signal (V_{Ref}) is represented in Fig.3.(c). The comparison of proposed topology with other recent topologies is given in Table.2.

III. SIMULATION AND EXPERIMENTAL RESULTS

The simulation and experimental verification of *CSCMLI* is carried out by using MATLAB/Simulink and *DSpace-1104* for pulse generation and circuit diagram is depicted in Fig.4. The simulation and experimental parameters values are listed in Table. 3. In simulation the input voltage is 320*V* and the capacitor ratings are 4700μF with voltage rating of 80V, these values are chosen based on the percentage of ripples in the capacitor voltage and switching frequency of the inverter.

TABLE. 3 PARAMETER USED IN SIMULATION AND EXPERIMENTAL SETUP

Parameters	Simulation	Experimental
DC Input voltage (V_{in})	320V	320V
Capacitor Rating (C_1,C_2)	80V,4700µF	80V,4700µF
R,L Load	150Ω,300mH	R-L load bank
Output Voltage (V_{out})	228V(V_{rms})	228V(V_{rms})
Output Current (I_o)	1.8A (I_{rms})	0.5A-1.8A (I_{rms})
Output Power	0.1kW-0.3kW	0.1kW- 0.4kW
Switching Frequency	50Hz, 2.5kHz	50Hz, 2.5kHz
Voltage THD	13.11%, 12.52%	13.95%, 13.1%

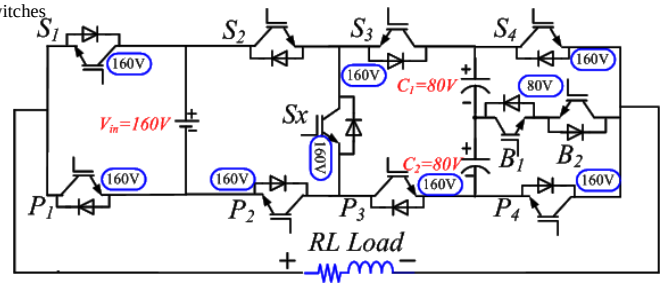

Fig.4 Simulated proposed nine level MLI with blocking voltage on the individual switches

The proposed inverter along with the modulation technique is verified in both high switching frequency (2.5 kHz) and fundamental switching frequency (50Hz) in simulation and experimental model. The corresponding switches are triggered by using parabolic modulation technique and the simulated results are captured as shown in Fig.5. The dynamic performance is simulated by varying the resistive-inductive load values from high-low-high as shown in Fig.5 (a) and the capacitor voltages are shown in Fig.5 (b), i.e the capacitor is independent of the load power factor. For motor drive applications, the high switching frequency is not preferred, so the proposed topology and modulation scheme is verified for low switching frequency of 50 Hz and waveforms are shown in Fig.5(c) and (d). In experimental setup, the semikron *IGBT SKM75GB063D IGBT* and *SKYPER-32-PRO-R* gate driver circuits are used. The dead time of 2µs is provided by using *RC* network. The input voltage (V_{in}) 320*V* is given through the direct DC supply and a variable *RL* load banks of 0.1*kW* to 0.4*kW* is used.

In the hardware, the high and low switching frequencies in PWM control with unity power factor are tested and waveforms are shown Fig. 6(a) and Fig.7 (a). The dynamic performance of proposed control and the inverter is explored in both high and low switching frequencies and the corresponding output voltage and current waveforms are shown in Fig.6 (b) and Fig.7(b). For dynamic performance the load values are gradually varied from high to low. For lagging power factor, the corresponding capacitor voltage waveform is shown in Fig.7(c). It is confirming that the proposed topology and parabola modulation technique is able to adopt for load variations. Further, the voltage THD value of proposed modulation technique is 12.52% and 13.1% for high and low switching frequency, respectively which is slightly lower than the other conventional PWM methods.

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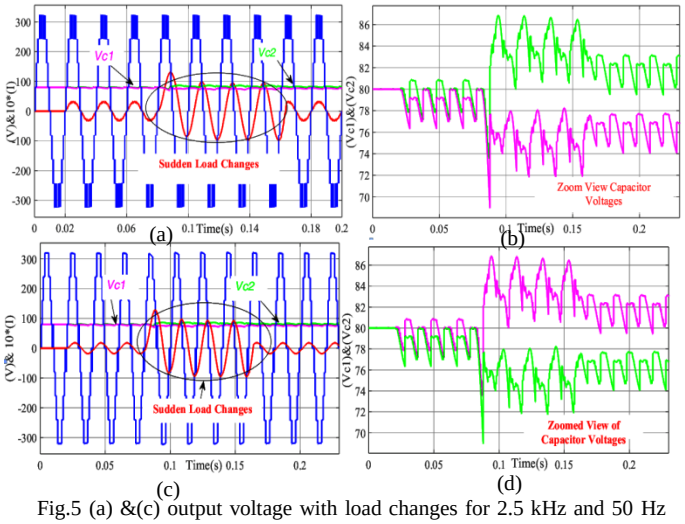

Fig.5 (a) &(c) output voltage with load changes for 2.5 kHz and 50 Hz switching frequency, (b) & (d) the capacitor voltage during load changes

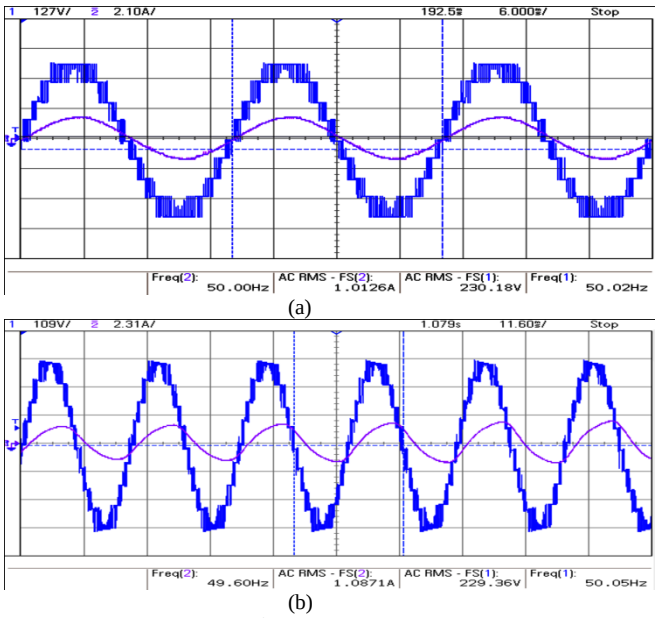

Fig.6 Experimental results of proposed nine level inverter with switching frequency of 2.5 kHz (a) static load with high load resistance value (b) varying load with high load inductance value

The sizing of capacitor is

$$C_1 = C_2 = \frac{I_{pk}}{\Delta V_C \times f_{sw}} \qquad (3)$$

In (3), voltage ripples (ΔV_C), switching frequency (f_{sw}), and the peak load current (I_{pk}) are chosen and the captured voltage waveforms are shown in Fig.7(c). Further to investigate the performance of modulation technique, the rms voltage and THDs are measured for various modulation indices and is listed in Table.4.

TABLE.4 THD COMPARISON OF VARIOUS MODULATION TECHNIQUES FOR SWITCHING FREQUENCY OF 2.5KHZ

Modulation Techniques		Ma=1.0		Ma=0.8		Ma=0.6	
		V_{rms}	THD%	V_{rms}	THD%	V_{rms}	THD%
Sawtooth PWM		225.8	14.32	188.2	17.24	143.8	25.44
Sinusoidal PWM	PD	226.7	13.66	189.5	16.99	145.3	24.36
	POD	226.4	13.46	189.7	16.81	145.3	24.30
	APOD	226.5	13.78	189.7	16.90	145.3	24.12
	Parabolic	228.4	12.52	189.3	15.66	146.0	22.61

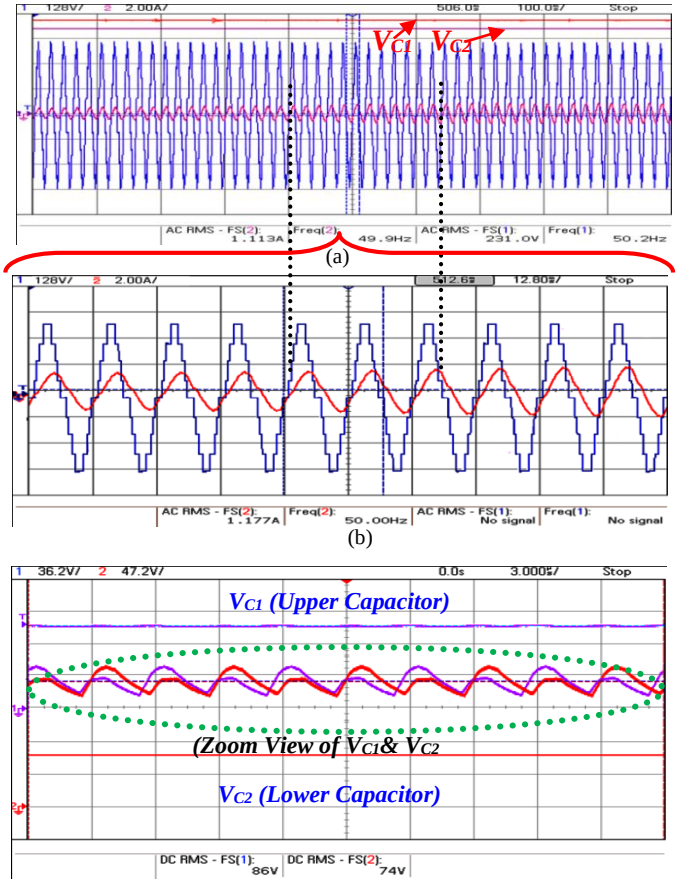

Fig.7 Experimental results for 2.5 kHz switching frequency (a) voltage and current for continuous load changes (b) zoomed view and (c) voltage across the capacitors C_1 & C_2

IV. CONCLUSION

A new voltage boost with self-voltage balancing across the capacitor in the nine level CSCMLI topology is proposed along with a new modified carrier signal. A single dc source is used and the output voltage is boosted twice *i.e* voltage gain is doubled. The voltage across each switch is limited to V_{in} which is the remarkable advantage of the proposed topology, because the number of active switches are reduced and this leads to low power losses. The capacitors voltages are not affected due to the load variations i.e capacitor voltages are independent of load power factor. Further, the proposed modulation technique is adaptable for both low and high switching frequency applications like a renewable energy power conversion system, AC drive applications, etc.

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